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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,562	09/05/2006	Hiroshi Itahara	41083	7244

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	

ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
08/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,562	ITAHARA, HIROSHI	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9-05-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

It is suggested to insert the continuing data in the first page, and line 1 of the specification.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 - 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaeger et al. (US Patent Number 5,253,272).

3. Regarding claim 1, Jaeger et al. discloses a power amplifying apparatus (fig. 3) , comprising: a distributing unit (34, fig. 3) that divides an input digital signal to a plurality of the input digital signals so as to distribute the input digital signals to a plurality of devices respectively (ADATA, BDATA are the plurality of data that is divided by the distribution unit); and a synthesizing unit that synthesizing output signals from the devices to output the synthesized output signal (col. 4, lines 56 – 68; col. 5, lines 41 – 49; col. 6, lines 3 - 8), wherein each of the devices includes: a delay regulating unit that regulates a delay amount of the input digital signal (col. 3, lines 43 – 57; col. 5, lines 30 - 39; col. 11, lines 5 – 10); a digital/analog converting unit (not shown) that converts the digital signal regulated by the delay regulating unit to an analog signal (as disclosed in the abstract and throughout the specification, Jaeger et al. distribute digital system,

thereby the system comprises a DAC that converts the digital data into analog converter)[see title, abstract, col. 3, line 43 to col. 4, lines 15); and an amplifying unit (74, fig. 4) that amplifies the analog signal to output the amplified analog signal to the synthesizing unit (col. 7, lines 15 – 26) .

4. Regarding claim 2, Jaeger et al. discloses a power amplifying apparatus (fig. 3) wherein the delay regulating unit includes a shift register (36, 38, fig. 3) in which the number of stages is variable(col. 43 – 57; col. 5, lines 30 - 39; col. 11, lines 5 – 10); and wherein the delay regulating unit adjusts the number of stages of the shift register to regulate the delay amount of the input digital signal (col. 43 – 57; col. 5, lines 30 - 39; col. 11, lines 5 – 10).

5. Regarding claim 3, Jaeger et al. discloses a power amplifying apparatus (fig. 3) further comprising an input clock control unit (40, fig. 3) that controls a phase of an input clock signal of the digital/analog converting unit of each of the devices (fig. 3; col. 52 - 60).

6. Regarding claim 4, Jaeger discloses a power amplifying apparatus (figs. 3, 4) wherein the delay regulating unit includes a digital filter (abstract; col.); and wherein the delay regulating unit adjusts a filter coefficient of the digital filter to regulate the delay amount of the input digital signal (fig. 4; paragraph bridging col. 6 and 7; col. 11, lines 30 – 36).

7. Regarding claims 5, 6, Jaeger et al. discloses a power combining system and method (fig. 3) , comprising: a distributing unit (34, fig. 3) that divides an input digital signal to a plurality of the input digital signals so as to distribute the input digital signals

to a plurality of devices respectively (ADATA, BDATA are the plurality of data that is divided by the distribution unit); and a synthesizing unit that synthesizing output signals from the devices to output the synthesized output signal (col. 4, lines 56 – 68; col. 5, lines 41 – 49; col. 6, lines 3 - 8); wherein each of the devices includes: a delay regulating unit that regulates a delay amount of the input digital signal (col. 3, lines 43 – 57; col. 5, lines 30 - 39; col. 11, lines 5 – 10); a digital/analog converting unit that converts the digital signal regulated by the delay regulating unit to an analog signal (as disclosed in the abstract and throughout the specification, Jaeger et al. distribute digital system, thereby the system comprises a DAC that converts the digital data into analog converter)[see title, abstract, col. 3, line 43 to col. 4, lines 15); and an amplifying unit (74, fig. 4) that amplifies the analog signal to output the amplified analog signal to the synthesizing unit (col. 7, lines 15 – 26), the power combining system, further comprising: a measuring unit that acquires at least one of an output power and a frequency characteristic of the synthesized output signal to measure a delay between the devices (figs. 3, 4; col. 4, lines 56 – 68; col. 5, lines 41 – 49; col. 6, lines 3 – 8; col. 11, lines 5 – 10)[the delay line provides the delay to the connecting lines, This delay is inherently calculated or measured]; and a control unit that controls the delay regulating unit so as to regulate the delay amount of the input digital signal based on the measured delay between the devices (col. 4, lines 20 – 44).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-

272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean Bruner Jeanglaude
Primary Examiner
July 23, 2007